HTM095P02 P-1

20V P-Ch Power MOSFET

F[illegible]

H[illegible]
E[illegible] A[illegible]
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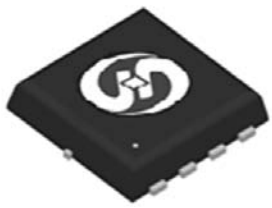
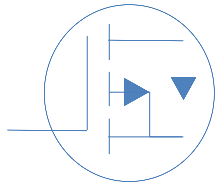
V_{DS}		-20	V
$R_{DS(on),typ}$	V_{GS}=-4.5V	7.8	mΩ
$R_{DS(on),typ}$	V_{GS}=-2.5V	10.3	mΩ
$R_{DS(on),typ}$	V_{GS}=-1.8V	14.5	mΩ
I_D (Sillicon Limited)		-15	A

A[illegible]

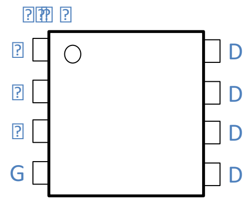
H[illegible] H[illegible] C[illegible]
DC[illegible]DC [illegible]

DF[illegible]





Part Number	Package	Marking
HTM095P02	DFN3*3	TM095P02



Absolute Maximum Ratings at T_j=25 (unless otherwise specified)

Parameter	Symbol	Conditions	Value	Unit
Continuous Drain Current (Silicon Limited)	I_D	T_A=25	-20	A
		T_A=70	-15	
Drain to Source Voltage	V_{DS}	-	-20	V
Gate to Source Voltage	V_{GS}	-	±8	V
Pulsed Drain Current	I_{DM}	-	-80	A
Avalanche Energy, Single Pulse	E_{AS}	L=0.1mH, T_C=25	11.25	mJ
Power Dissipation	P_D	T_A=25	2.5	W
Operating and Storage Temperature	T_J, T_{stg}	-	-55 to150	

Absolute Maximum Ratings

Parameter	Symbol	Max	Unit
Thermal Resistance Junction-Ambient	$R_{\theta JA}$	50	/W
Thermal Resistance Junction-Case	$R_{\theta JC}$	6	/W

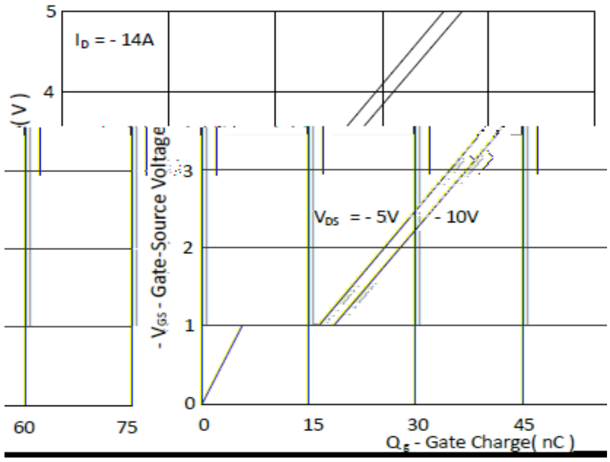
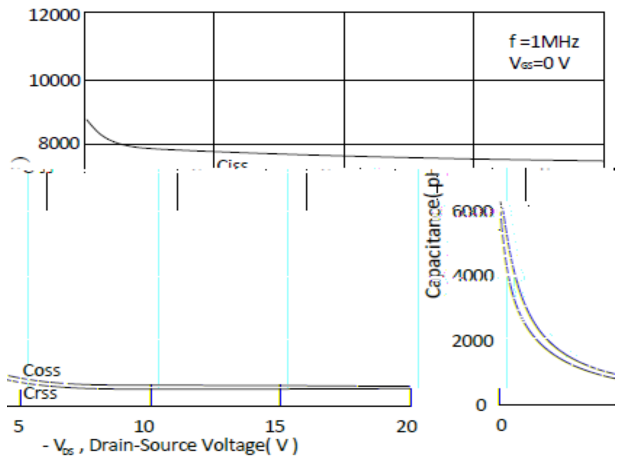
Figure 6. Typical Gate-Charge vs. Gate-to-Source Voltage	Figure 7. Typical Capacitance vs. Drain-to-Source Voltage
	

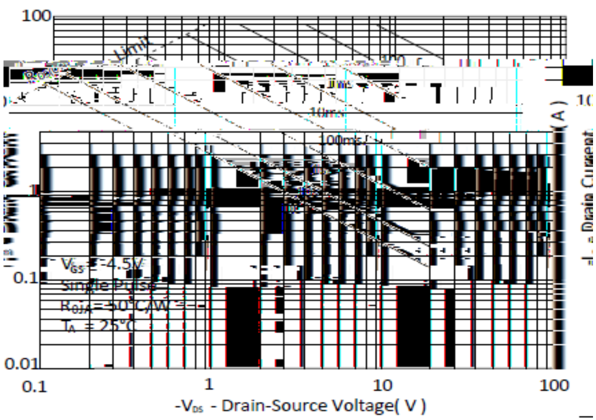
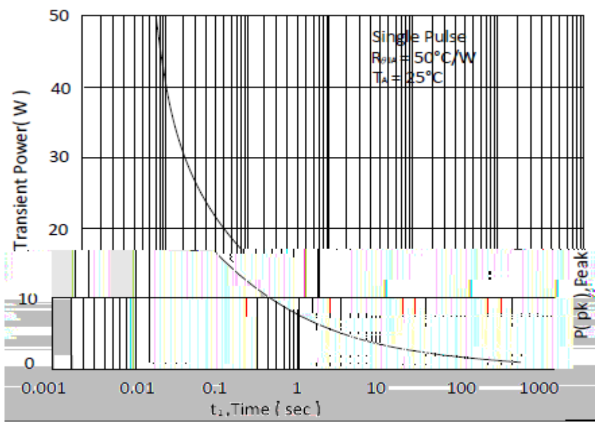
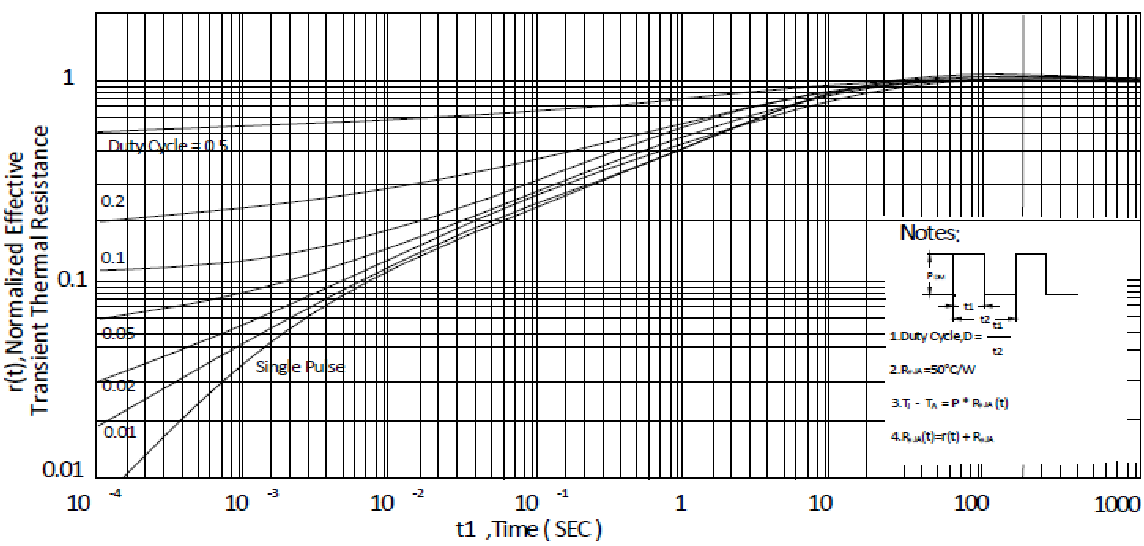
Figure 8. Maximum Safe Operating Area	Figure 9. Single Pulse Maximum Power Dissipation
	

Figure 10. Normalized Maximum Transient Thermal Impedance, Junction-to-Ambient



Inductive switching Test	

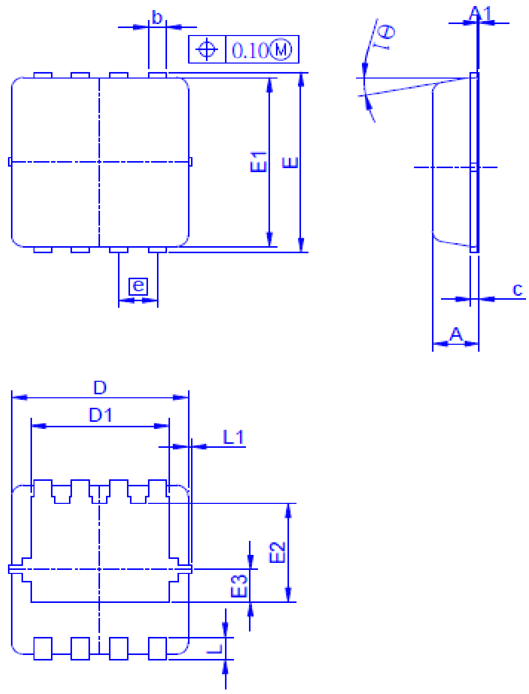
Gate Charge Test	

Uclamped Inductive Switching (UIS) Test	

Diode Recovery Test	

Package Outline

DFN3*3, 8leads



Dimension in mm

Dimension	A	A1	b	c	D	D1	E	E1	E2	E3	e	L	L1	Θ1
	0.30		0°	Min.		0.70	0	0.24	0.10	2.95	2.25	3.15	2.95	1.65
.575 0.65	0.40	0.13	10°	Typ.		0.80		0.30	0.152	3.00	2.35	3.20	3.00	1.75 0.
	0.50		12°	Max.		0.90	0.05	0.37	0.25	3.15	2.45	3.40	3.15	1.96